IN THE CLAIMS:

Please amend claims 13, 21 and 22, and add new claims 23 and 24, as follows.

Claims 1-5 (Canceled).

6. (Previously Presented) A memory device, comprising:

a switch array comprising a plurality of first switches for connecting a lower byte region of a data I/O buffer to a lower byte region of a sense amplifier array, a plurality of second switches for connecting the lower byte region of a data I/O buffer to an upper byte region of the sense amplifier array, and a plurality of third switches for connecting an upper byte region of the data I/O buffer to the upper byte region of the sense amplifier array; and

a switch controller for receiving external control signals to control activation of the data I/O buffer and on/off operations of the first through the third switches,

wherein the switch controller turns on the first switch and activates the lower byte region of the data I/O buffer connected to an I/O port when a lower byte signal included in the external control signals is activated, and turns on the third switch and activates the upper byte region of the data I/O buffer connected to an I/O port when an upper byte signal included in the external control signals is activated.

7. (Previously Presented) A memory device, comprising:

a switch array comprising a plurality of first switches for connecting a lower byte region of a data I/O buffer to a lower byte region of a sense amplifier array, a plurality of second switches for connecting the lower byte region of a data I/O buffer to an upper byte region of the sense amplifier array, and a plurality of third switches for connecting an upper byte region of the data I/O buffer to the upper byte region of the sense amplifier array; and

a switch controller for receiving external control signals to control activation of the data I/O buffer and on/off operations of the first through the third switches,

wherein the lower byte region of the data I/O buffer is connected to an I/O port, the upper byte region of the data I/O buffer is not connected to an I/O port, and a control signal included in the external control signals is provided through a terminal pin connected to the upper byte region of the data I/O buffer.

8. (Original) The memory device according to claim 7, wherein the switch controller activates the first switches when the control signal inputted through the terminal pin is "0", and the second switches when the control signal inputted through the terminal pin is "1".

9. (Previously Presented) The memory device according to claim 6, wherein the switch controller inactivates the upper byte region of the data I/O buffer and activates the second switches if a control signal inputted through a terminal pin connected to the upper byte region is "1", and activates the first switches if the control signal inputted through the terminal pin is "0" when a byte signal included in the external control signals is activated, and

the switch controller turns on the first switches and then activates a lower byte region of the data I/O buffer if a lower byte signal included in the external control signals is activated, and turns on the third switches and then activates an upper region of the data I/O buffer if an upper byte signal included in the external control signal is activated when the byte signal is inactivated.

Claims 10-12 (Canceled).

13. (Currently Amended) A memory device, comprising:

a switch array comprising a plurality of first switches for connecting a lower byte region of a data I/O buffer to a lower byte region of a sense amplifier array, a plurality of second switches for connecting the lower byte region of a data I/O buffer to an upper byte region of the sense amplifier array, and a plurality of third switches for connecting an upper byte region of the data I/O buffer to the upper byte region of the sense amplifier array; and

a switch controller for receiving external control signals to control activation of the data I/O buffer and on/off operations of the first through the third switches,

wherein the memory device is a ferroelectric memory device having a bitline structure comprising a main bitline and a plurality of sub bitlines <u>each connected to a plurality of memory cells, wherein sensing voltage at the main bitline is induced by sensing current which is controlled by voltage at one of the plurality of sub bitlines according to a data stored in one of the plurality of memory cells</u>.

Claims 14-17 (Canceled).

18. (Previously Presented) A memory device that processes data by two bytes comprising a lower byte and an upper byte that is capable of operating with a system that processes data by one byte, comprising:

a plurality of data pads connected to the system;

a data input/output buffer coupled to the plurality of data pads and comprising a lower byte region and an upper byte region;

a circuit that stores data of the lower byte region of the data input/output buffer to either an upper byte region or a lower byte region of data storing portion depending upon an external control signal received on a data pad coupled to the upper byte region of the data input/output buffer.

Claim 19 (Canceled).

20. (Previously Presented) The memory device according to the claim 18, wherein the external control signal is a least significant bit of an address signal.

21. (Currently Amended) A system comprising the memory device ~~according to the claim 6~~, wherein the memory device comprising:

a switch array comprising a plurality of first switches for connecting a lower byte region of a data I/O buffer to a lower byte region of a sense amplifier array, a plurality of second switches for connecting the lower byte region of a data I/O buffer to an upper byte region of the sense amplifier array, and a plurality of third switches for connecting an upper byte region of a data I/O buffer to the upper byte region of the sense amplifier array; and

a switch controller for receiving external control signals to control activation of the data I/O buffer and on/off operations of the first through the third switches,

wherein the switch controller turns on the first switch and activates the lower byte region of the data I/O buffer connected to an I/O port when a lower byte signal included in the external control signals is activated, and turns on the third switch and activates the upper byte region of the data I/O buffer connected to an I/O port when an upper byte signal included in the external control signals is activated.

22. (Currently Amended) A system comprising the memory device ~~according to the claim 7~~, wherein the memory device comprising:

a switch array comprising a plurality of first switches for connecting a lower byte region of a data I/O buffer to a lower byte region of a sense amplifier array, a plurality of second switches for connecting the lower byte region of a data I/O buffer to an upper byte region of the sense amplifier array, and a plurality of third switches for connecting an upper byte region of a data I/O buffer to the upper byte region of the sense amplifier array; and

a switch controller for receiving external control signals to control activation of the data I/O buffer and on/off operations of the first through the third switches,

wherein the lower byte region of the data I/O buffer is connected to an I/O port, the upper byte region of the data I/O buffer is not connected to an I/O port, and a control signal included in the external control signals is provided through a terminal pin connected to the upper byte region of the data I/O buffer.

23. (New) A method for operating an electronic memory device that processes data by two bytes having a data buffer comprising an upper byte portion and a lower byte portion to enable the electronic memory device to operate with a system bus that processes data by one byte, comprising:

receiving an address bit on an input for the upper byte portion of the data buffer; and

using the address bit received on the input for the upper byte portion of the data buffer to control the output and input of data from/to the system bus.

24. (New) A method for storing data provided by a system that processes data by one byte in an electronic memory device that stores data by two bytes associated with an address in the form of an upper byte portion and a lower byte portion, comprising the steps:

receiving a data byte and a one-byte address for the data byte from the system, the one-byte address having a least significant bit, wherein the least significant bit is received as an input to a upper byte portion of a data input/output; and

storing the received data byte to either the upper byte portion or the lower byte portion associated with the address in response to the least significant bit.